ABSTRACT OF THE DISCLOSURE

A packet communication apparatus processes consecutively transmitted fixed-length packets. The apparatus includes a storage circuit, a first processing circuit which accesses the storage circuit for processing data obtained from each of the packets, and a second processing circuit which accesses the storage circuit for processing data stored in the storage circuit. The apparatus further includes an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of the packets. Specifically, the allocation circuit allocates a first time of the packet processing time to the first processing circuit for accessing the storage circuit and a second time of the packet processing time to the second processing circuit for accessing the storage circuit. The first time and the second time are prevented from overlapping with each other.